A 6-Bit Two-Channel TI ADC in Si-Ge HBT BICMOS Technology

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***Abstract* – This paper presents design steps of a 6-bit two-channel time-interleaved (TI) ADC in 0.25µm Si-Ge HBT BiCMOS technology. Two 6-bit flash ADC cores are used in both time-interleaved channels. In digital parts of the design, standard CMOS logic gates are preferred since a low power consumption value is one of the main targets of this work. Transistor sizes are selected carefully to be able to obtain as high as possible speed performance, which is another main goal of this study. The main core design blocks of the complete TI ADC are sample/hold circuit, 6-Bit Flash ADC, a 6-bit 2x1 digital multiplexer, and a control pulse generator. BiCMOS analog comparator architecture is preferred in the analog part of flash ADC since BiCMOS technology combines the advantages of CMOS and Bipolar technologies. The power consumption value is 653 mW under a single DC power supply voltage of 3.3V. The simulation results include 7Gs/s sampling rate, 0,174 LSB of INL and 0,113 LSB of DNL values. The simulation results are compared to similar works in the literature. For the time being, the complete design is realized using Cadence IC design platform in schematic level only. However, the physical layout design and post-layout simulation steps are ongoing research of us.**

***Keywords* – TI ADC, Si-Ge HBT BICMOS, Flash ADC, VLSI**

I. INTRODUCTION

IN recent years, high speed and low power analog-to-digital converters (ADC) have important role in new generation signal processing and communication systems. There are several different types of ADC architectures in the literature, depending on the type of application. Typically, the serial ones have very high resolution, yielding higher accuracy whereas parallel ones operate at very high frequencies but have relatively low resolution. The flash ADC architecture is known as the fastest one among high speed ADCs since the conversion speed is only one clock cycle.

In the last decade, however, popular ADC architectures to satisfy the requirements of new generation RF communication systems are pipeline and time interleaved (TI) type of ADCs. The performance of TI-ADC is affected by mismatches among the interleaves, especially the mismatches of sampling time, gain and offset [1]. On the other hand, pipeline ADCs require calibration and correction logic additionally. To obtain desired resolution and accuracy levels are tedious work. Therefore, timing of controlling clock pulses for more than two pipelining stages are very critical for pipeline ADC case. For this reason, TI -ADC architecture is chosen in this study.

TI-ADC is used to increase the sampling rate of a specific core ADC, which is either Flash or SAR architecture in general. If the speed is the major concern, then Flash ADC core is inevitable as explained above. A traditional TI ADC architecture consists of N number of Sample and Hold (S/H) circuits, N number of core ADCs, a digital multiplexer and a digital pulse generator to produce the critical timing clock signals as shown in Figure 1. Here, N indicates the number of interleaving channels.

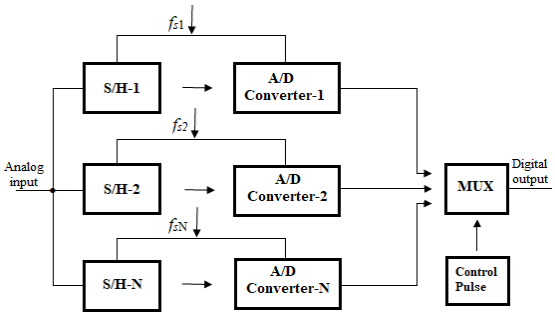


Figure 1: Block diagram of N–channel TI ADC

The sampling clock phases of each ADC cores are very important in TI-ADCs as mentioned above. The sampling rate of a TI ADC is given by F_s=N/T, where N is the number of channels and T is the minimum sampling period of a single ADC core. For instance, if four-channel TI_ADC is designed, and maximum sampling rate of each core ADC is assumed as 2Gs/s, then the final TI-ADC is supposed to have a sampling rate of 8GS/s. Timing diagram of an N channel TI-ADC is depicted in Figure 2 [2].

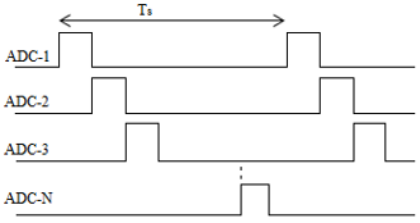


Figure 2: Timing diagram of N–channel TI ADC

The S/H circuits in TI ADC architecture are used to create an analog de-multiplexer circuit, which decides which ADC channel will work in which timing interval. Because the analog input signal is only one signal. The binary converted digital output data for a quantized input level is obtained from the core ADC outputs. Then, each ADC channel output is connected to

a specific digital multiplexer input. The resolution of the multiplexer inputs and the core ADCs are the same. The control pulse generator produces the sampling clock pulses at the input and the select control pulses of the digital multiplexer. The multiplexer is responsible for transferring the binary outputs of ADC cores in correct order to the final digital output port [3]. The timing and the synchronization issue of this operation is the most critical and difficult part of a TI-ADC design in general. In this study, a BiCMOS comparator based 6-bit Flash ADC core is decided for each channel to design a 6-bit TI-ADC in 250 nm BiCMOS technology using Cadence IC Design tools.

The rest of the paper is organized as follows: Section II describes all design steps of the proposed BiCMOS TI ADC. The circuit schematics of all design blocks are shown and explained in detail. The simulation results are given and discussed in Section III. Finally, Section IV concludes the study.

II. Design Steps of The Proposed Time Interleaved ADC

The proposed TI-ADC consists of the following core designs: S/H circuit, 6-bit Flash ADC, 2x1 multiplexer having 6-bit inputs and pulse generator. The following sub-sections describe them in detail.

A. *The Sample and Hold Circuit*

In this study, a simple CMOS analog switch with a hold capacitor at the output is used as a S/H circuit core as shown in Figure 3. The S/H circuit affects the speed performance and the accuracy of a TI-ADC. In fact, very high performance BiCMOS S/H circuits are available in the literature. However, the design of them is not an easy task. S/H circuit is responsible for sampling the analog input signal at a specific time and holding the corresponding input voltage level across the hold capacitor at the output. There are two S/H circuits in this work since the number of channel is chosen as two.

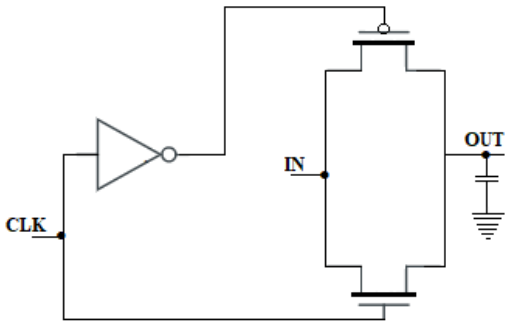


Figure 3: The sample and hold circuit

B. *The Flash ADC Core*

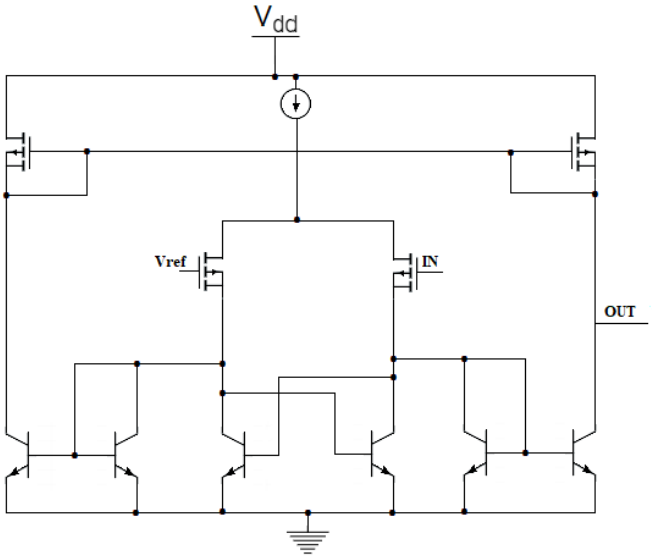
Full-flash ADC works in fully parallel fashion which makes it the fastest one among other ADCs. It consists of two main blocks as the analog part and the digital part. The analog part consists of a resistor array to produce quantization voltage levels for comparison purpose at the comparator array inputs, and comparator array. In this study, 6-bit resolution is aimed. Therefore, 64 number of resistors and 63 number of BiCMOS comparators form the analog part of the Flash ADC core of the proposed TI-ADC. The block diagram of the flash ADC core is shown in Figure 4.



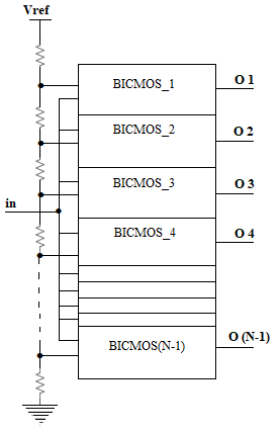
Figure 4: The Flash ADC block diagram

a) *The BICMOS Comparator Circuit*

The comparators are the most important parts of Flash ADC architectures since their throughput and power consumption values are almost entirely depend on the comparator performance. In this study, a silicon-Germanium (Si-Ge) technology is chosen for its speed advantage over fully silicon CMOS circuits.



(a)



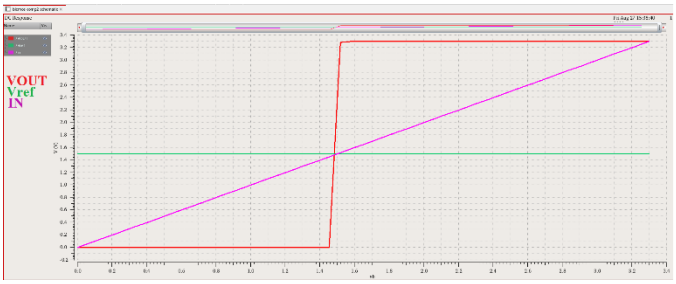
(b)

Figure 5: (a) The BICMOS comparator (b) The BICMOS comparator array

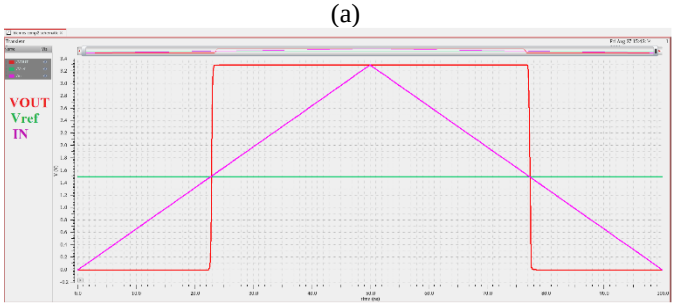
The BiCMOS comparator schematic used in this work is shown in Figure 5(a). This circuit is called as dynamic latch

comparator with push-pull output stage in [4]. However, optimum device sizes are reached after several transient simulations to obtain a higher speed and gain. The power supply voltage is a single 1.5 V. The complete comparator array structure is depicted in Figure 5(b).

The DC voltage transfer characteristic and transient analysis result are shown in Figure 6(a) and 6(b), respectively. The transient results and DC results of the complete analog part are also depicted in Figure 7(a) and Figure 7(b), respectively. As can be seen, 63 of transition levels are obtained almost with same distances in between.

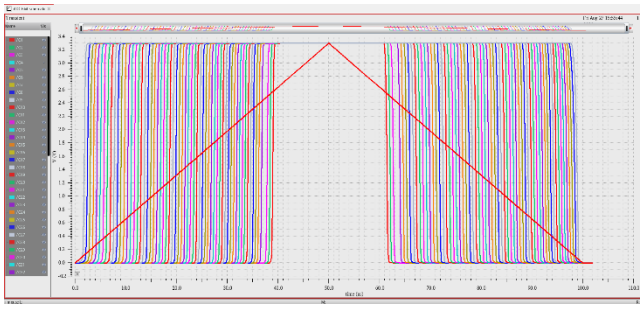


(a)

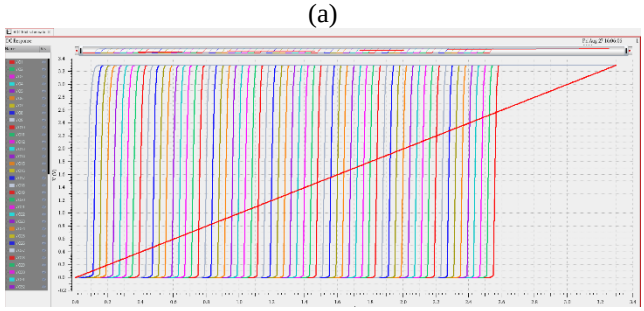


(b)

Figure 6: (a) DC simulation result of the BiCMOS comparator (b) Transient simulation result



(a)



(b)

Figure 7: (a) Transient results of the complete comparator array (b) DC analysis results

b) The Dynamic Latch Circuit

The dynamic latch array is the first stage of digital part of Flash ADC. It keeps the logic output of the comparator array outputs (namely thermometer code) for a while to relax the rest part of the digital part until the final binary output is obtained. Since the analog input signal is continuous, the digital code belongs to an instantaneous input voltage can never be obtained at the same time due to the propagation delay of the digital part. Therefore, a dynamic latch circuit is necessary for ADC designs in general. The thermometer code is kept during the controlling CLK is logic "0". The period of the latch clock pulse defines the digital sampling rate of the Flash ADC. The circuit schematic of the dynamic CMOS inverter is shown in Figure 8 [5].

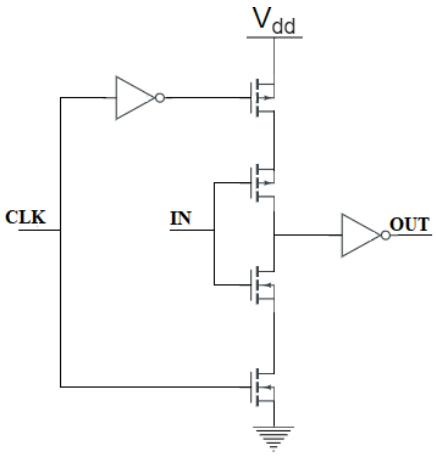
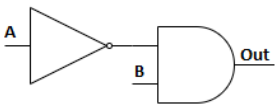


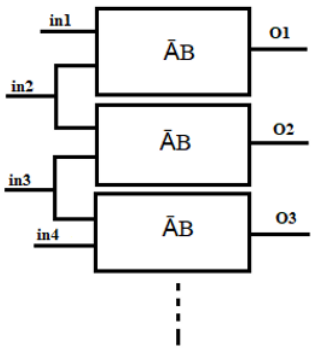
Figure 8: The dynamic latch circuit schematic

c) The 1-of-N Decoder Block

The thermometer code is converted to so-called 1-of-N code, which is necessary for the final stage, PLA-ROM circuit. The outputs of the 1-of-N decoder block shown in Figure 9 include only one logic "1", but the rest is all logic "0". This array block has a unit cell realizing F= $\bar{A}B$ function as shown in Figure 9(a).



a)



b)

Figure 9: (a) $\bar{A}B$ logic circuit (b) 1-of-N decoder block

d) PLA-ROM Circuit

The PLA-ROM circuit shown in Figure 10 is responsible for converting 1-of-N code to n-bit binary code. The final 6-bit binary output data of the Flash ADC is obtained at the outputs of this circuit. The basic cell of this structure is a PMOS load inverter. There are 6 columns and 63 rows here. NMOS transistors on each row are arranged according to the corresponding digital output code. The CMOS inverters at the output are used not only for logic inversion but also for gain boosting and buffering purposes. The complete schematic of the Flash ADC core is shown in Figure 11 after realizing each sub-blocks.

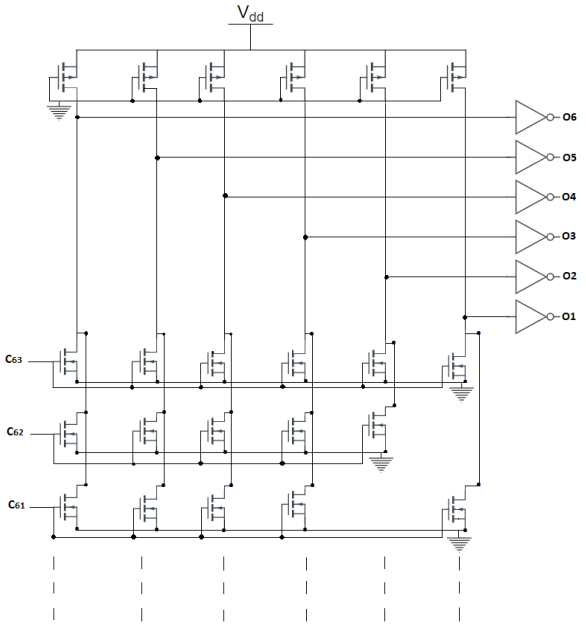


Figure 10: The PLA-ROM circuit

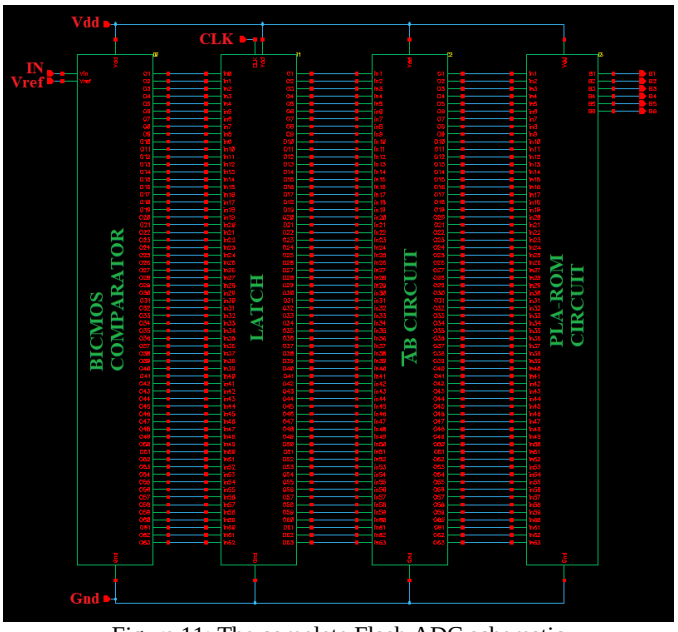


Figure 11: The complete Flash ADC schematic

C. The 2x1 Multiplexer Circuit

There are six 1-bit 2x1 CMOS multiplexers used in this block. The schematic of each 1-bit 2x1 multiplexer unit is shown in Figure 12 [6]. Timing of the select terminal of this multiplexer block is very important for a proper operation. The digital multiplexer block of the complete TI -DC must work at faster speed than that of each Flash ADC core. The control pulse generator circuit produces the system clock pulses, and coordinates the all critical timing and synchronization process.

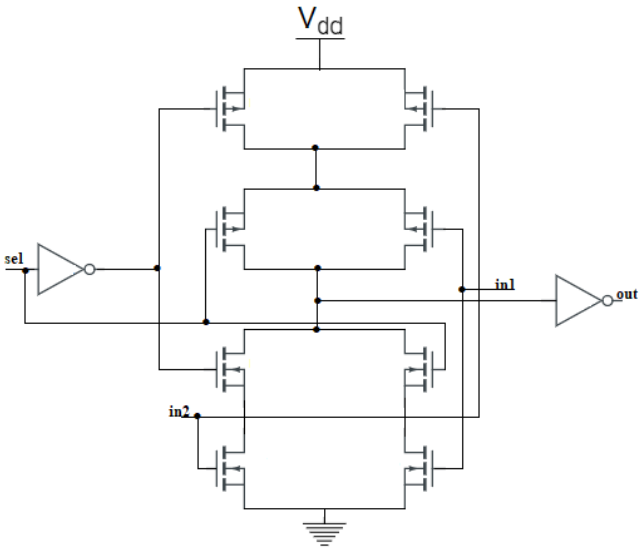


Figure 12: The multiplexer circuit [6]

D. Pulse Generator

The sampling control pulses of the analog de-multiplexer unit, the latch clock signals and select control pulse of the digital multiplexer are generated by this unit. The schematic of the pulse generator shown in Figure 13 is chosen from the literature [7], and the transistor aspect ratios are modified inside it. The speed performance of this circuit must be satisfying. Although the circuit schematic is simple, to obtain non-overlapping clock pulses with critical time delays is a tedious work. If the number of channels are increased, then this task become more difficult. There are four and even 8 channel TI-ADC examples can be found in the literature. Therefore, controlling pulse generation schemes are different in general. After all sub-blocks of the TI-ADC are finished, they are integrated carefully to realize the complete TI-ADC. The complete schematic of the 6-bit two-channel BiCMOS Flash ADC is depicted in Figure 14.

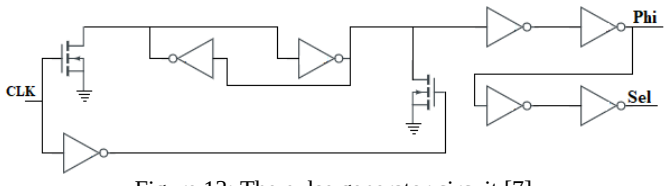


Figure 13: The pulse generator circuit [7]

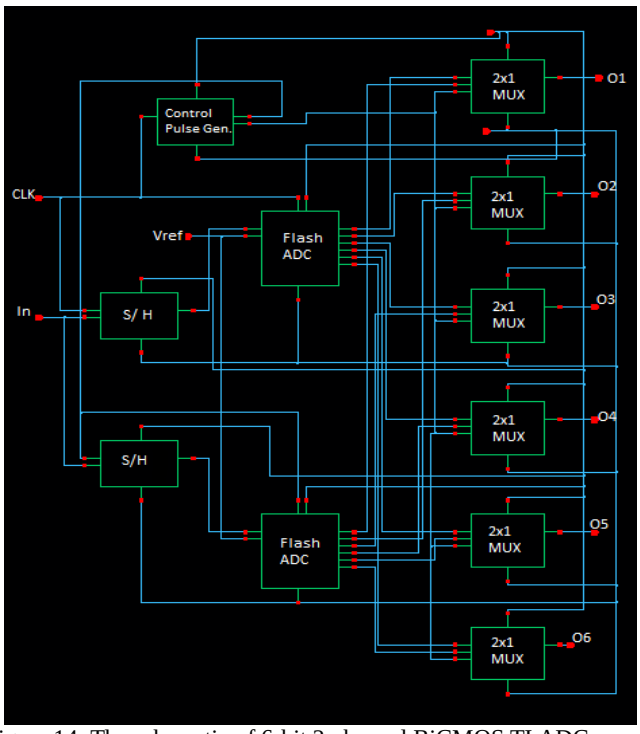


Figure 14: The schematic of 6-bit 2-channel BiCMOS TI ADC

III. Simulation Results

Schematics and simulations of the design are conducted using 0.25µm Si-Ge HBT BICMOS process parameters in Cadence IC Package Platform. Figure 15 and Figure 16 shows the transient simulation results of Flash ADC core and the complete TI ADC, respectively. As seen, there is almost no missing output code even for TI-ADC.

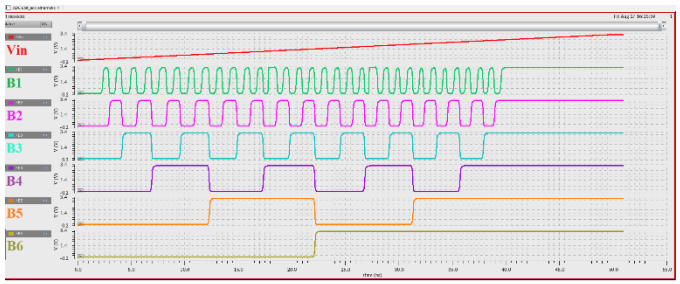


Figure 15: Transient results of the Flash ADC core

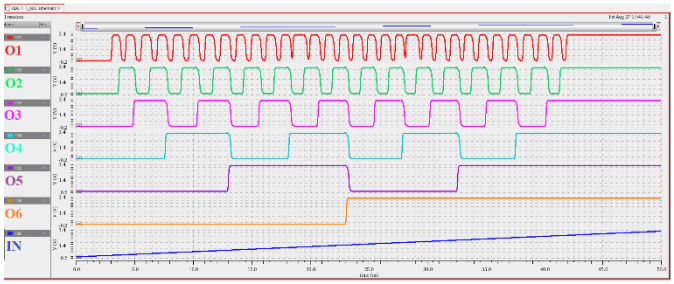
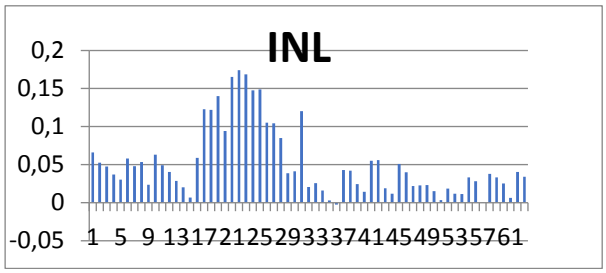
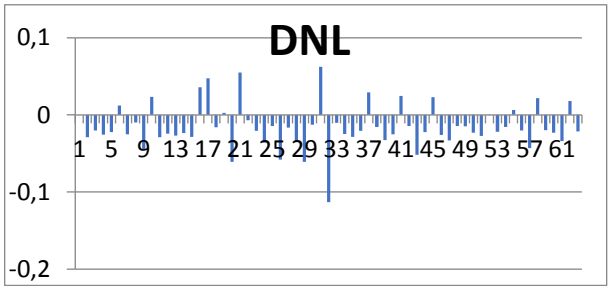


Figure 16: Transient results of the 6-bit 2-channel TI ADC

Figure 17 (a) and (b) shows the INL and DNL plots, respectively. The worst case INL value is 0.174 LSB, while DNL value is -0.113 LSB. Since all of the non-linearity measures are below 0.5 LSB, a monotonic converter operation is obtained. The design summary and a performance comparison is done in Table 1.



(a)



(b)

Figure 17: (a) INL Plot ,(b) DNL Plot

Table 1: Performance summary and comparison of the proposed TI-ADC

Parameters	This work	[2]	[8]	[9]
Design Technology	0.25µm Si-Ge HBT	0.25µm CMOS	0.65 µm CMOS	0.18 µm Si-Ge BICMOS
Resolution (bit)	6	4	6	6
Supply Voltage(V)	3.3	±1.5	1.5	3.3V-4.5V
INL (LSB)	-0.0022/ 0.174	+0.01/ -0.44 (f_{in}=100 MHz)	-0.4/0.7	-0.4/0.4
DNL (LSB)	-0.113/ 0.062	+0.26/ -0.22) (f_{in}=100 MHz)	-0.5/0.6	-0.2/0.2
Power Consumption (mW)	633.4	270	435	8.5W
Sampling Frequency (GHz)	7	10	16	30
Channel count	2	4	8	4
Core ADC	BICMOS Flash	CMOS Flash	CMOS Flash	SAR

IV. Conclusions And Future Works

In conclusion, a 6-bit TI-ADC was realized in 250nm Si-Ge HBT BiCMOS technology. A BiCMOS Flash ADC core was chosen in each interleaving channel. Cadence IC design platform was used during design and simulation processes. The

simulation results include 633,4 mW of ac power at 7GS/s operation under 3.3V power supply voltage, 0.74 LSB of INL, -0.113 LSB of DNL. When compared to other similar designs in the literature, this work is better in terms of linearity measures. The power consumption is lower than that of [9], but higher than others due to relatively higher supply voltage and Si-Ge HBT usage in the analog part. The sampling rate is lower than others since the number of channel is only two. As a future work, more ac performance measures will be obtained such as SNR and ENOB values. Also, post layout simulations will be conducted after completing the physical layout of the design. Moreover, the number of channel can be increased to four to obtain a higher sampling rate, which will require design of a new pulse generator circuit. In fact, this task requires a very high performance S/H or track and hold (T/H) amplifier circuit designs such as in [10]. Also, it is believed that more HBT usage in other sub-blocks as well in addition to the comparator circuit will increase the speed performance. It should be noted here that this work was the first attempt of an ADC design using Si-Ge BiCMOS technology of our VLSI research team.

V. REFERENCES

[1] F. Solis, A. F. Bocco, D. Morero, M. R. Hueda, B. T. Reyes, "Background Calibration Techniques of time interleaved ADC for optical coherent receivers using error backpropogation techniques", *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*,2020

[2] O. Aytar, A. Tangel, E. Afacan, "A 10 GS/s time-interleaved ADC in 0,25 micrometer CMOS technology", *Journal of ELECTRICAL ENGINEERING, VOL 68, NO6, 415-424*,2017.

[3] L. B. Yurekli, E. Akdere, A. Tangel, "130 nm CMOS Teknolojide 2 Kanallı Zaman Ayrışmalı ADC Tasarımı", *ELECO-2018, pp.242-248*, Bursa,Turkey ,2018.

[4] B. R. Sissons, "Silicon Germanium BİCMOS Comparator Designed for Use in An Extreme Environment Analog to Digital Converter," MsC thesis dissertation, University of Arkansas, May 2017.

[5] Y. Talay, O. Aytar "4 Bit Flash Tabanlı Zaman Sayısal Dönüştürücü Tasarımı" *Düzce Ünversitesi Bilim ve Teknoloji Dergisi, 7 52-62*, 2019.

[6] T. Dua, A. Rajput, "2:1 Multiplexer Using Different Design Styles: Comparative Analysis", *Journal of Advancements in Robotics*, vol.7 no 3, pp . 2455-1872, 2020.

[7] B.Nowacki, N. Paulino, J. Goes, "A Simple 1 GHz Non-Overlapping Two-Phase Clock Generators for SC Circuits", *20th International Conference "Mixed Design of Integrated Circuits and Systems*, Gdynia, Poland, June 20-22, 2013.

[8] C. Huang, C. Wang, J. Wu, "A CMOS 6-Bit 16-GS/s Time-Interleaved ADC Using Digital Background Calibration Techniques," *in IEEE Journal of Solid-State Circuits, vol. 46, no. 4, pp. 848-858,* April 2011.

[9] X. Zhui, D. Wu, L. Zhou, Y. Huang, J. Wu, X. Liu, "A four-channel time-interleaved 30-GS/s 6-bit ADC in 0.18 μm SiGe BiCMOS technology", *Science China*, vol. 60, Dec. 2017

[10] H. Ding, D. Wu, X. Zheng, L. Zhou, T. Chen, F. Lv, J. Wang, B. An, J. Wu, X. Liu, "A Low-Distortion 20 GS/s Four-Channel Time- Interleaved Sample-and-Hold Amplifier in 0.18 μm SiGe BiCMOS" *Electronics*, vol. 9(20), 2020.