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A High Voltage PIN Diode Design on SOI Substrate

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Abstract

This study is summary of the design optimization steps for a high voltage lateral silicon PIN diode on SOI substrate. The process simulations are realized using TCAD-SENTAURUS-SPROCESS design platform. The main purpose is to increase the reverse breakdown voltage of the PIN diode as high as possible. The design optimization process includes not only the chemical fabrication process details (such as doping concentration levels, dose amounts of the implants, temperature set values, duration of annealing or drive in processes) but also geometrical dimensions (such as length and thickness values of the layers). After the process simulations are completed, the electrical simulations are done using TCAD-SDEVICE platform to see the results. Finally, the design details of a PIN diode having a breakdown voltage of 600 V are reached. The scientific contribution of the paper is the proposed application of the well-known RESURF technique with field plate to increase the lateral breakdown voltage of silicon PIN diode. Also, a stepped implant structure is preferred on the cathode side. The paper includes most of the intermediate results and discussions of the optimization steps conducted during the research. The transient and ac sdevice electrical simulations are also completed but are not included in this paper.

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Keywords: PIN Diode; SOI; TCAD Sentaurus; Semiconductor Process Simulations; High Voltage Semiconductor Devices.

1. Introduction

PIN diodes are semiconductor devices used as variable resistors working at RF and microwave frequencies. They have very small resistor values in a specific frequency range even under very small bias currents. Therefore, these devices are commonly used as switching devices to control RF signals. [1]. While working as a switch or attenuator,

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they do not add any distortion to the signal when controlling RF signal level [2]. PIN structures are also popular in power electronic applications such as high voltage rectifier circuits. High power silicon diodes are also used in several RF applications up to 12 GHz typically. DC reverse breakdown voltage values of PIN diodes lie between 100V and 400V in typical commercial devices. They are also used as 3 terminal LPF broadband shunt structure in RF circuits [3]. A high breakdown voltage and low thermal resistance of a PIN diode provide peak power handling [4]. High voltage PIN diodes are also used as high voltage attenuator or limiter in RF circuits.

There are different fabrication technologies for PIN diodes. One of the popular techniques is so called SOI (Silicon-on-Insulator) technology. The SOI technology is preferred for high power integrated circuits since it has advantages of super isolation, low power loss, high speed and low leakage currents [5], [6]. In the literature, there are several studies and example papers related to high voltage devices, especially LDMOS realizations such as [5], [6], [7], [8], [9], [10], [11]. In fact, an SOI substrate usage only is not enough to obtain high enough reverse breakdown voltage values for high voltage applications. Therefore, several techniques have been developed and advertised in the literature to improve the reverse breakdown voltage capability of SOI devices.

Some of the well-known techniques when designing high voltage semiconductor devices are Reduced Surface Field Effect (RESURF) [8], Double RESURF [10], [12], isolation trenches [8], [11], Enhanced Dielectric Layer Field (ENDIF) [5]. RESURF technique is used for high voltage SOI devices to reduce electric field both in vertical and horizontal directions. This technique is usually preferred for high voltage PN, PIN junctions, and especially for designing LDMOSFETs. In SOI based PIN designs, SOI substrate itself can behave as an insulating field plate. In this case, when the diode is reversed biased, the vertical component of the electric field applied across the oxide induces a depletion region extending through the SOI layer [5]. This results in a large lateral depletion width and low horizontal component of electric field [5]. An example realization of PIN device having reverse breakdown voltage of 700 V in thin SOI substrate is presented in the literature [7].

A similar case study is also conducted and will be presented in detail here. However, the proposed design uses the field plate technique not in designing an LDMOS but in designing a high voltage PIN diode in SOI substrate. To prove the effect of field plate usage, several preceding case studies are conducted without using resurf technique with field plate. The selected design parameters to be optimized during TCAD process simulations are listed below:

1) Amount of implant doses
2) Doping concentration levels
3) Annealing temperature value and related timing after implant process
4) Final drive in temperature and related timing
5) Thickness of the I layer and the other layer geometries
6) Length of the layer and plate geometries

Please note that throughout the research, the design steps are numbered consecutively as soi-pin1,soi-pin2,…,soi-pin7. However, in this paper, only some of them having important results are mentioned here.

The paper is organized as follows: Section-2 presents sprocess simulation results and related discussions of the selected designs. The selected designs are called as SOI-pin5, SOI-pin6, SOIpin6-thin, SOI-pin7 respectively. Please note that in all figures showing the sprocess simulation results throughout this paper, X represents the length in X-direction in micron unit, Y represents the length in Y-direction (i.e depth) in micron unit in the wafer. Section-3 is the conclusion part, in which process parameters of the final optimized design are given.

2. Simulation Results and Discussions

In this section, the related critical fabrication parameters used during sprocess simulations are given on the related Figures.

2. 1 SOI-pin5 results

The plot depicted in Fig. 1 shows the sprocess simulation result of SOI-pin5. Fig. 2 shows the sdevice DC reverse bias simulation result, on which the diode reverse breakdown voltage (BV) is observed as 345 V. The related forward bias DC simulation result is given in Fig. 3, on which the built-in-potential (Vbi) value is seen as 0.85 V

approximately. In this paper, forward bias I-V characteristic plot of SOI-pin5 is given only due to minor changes observed on Vbi values of the other process simulations. In this specific design, the final drive in duration is increased to 180 minutes. Unfortunately, this yields reduction of BV to 240 V. Also in other design attempts (such as in the design called SOI-pin6), additional oxide regions are put either on the surface or underneath the surface, but no improvement is obtained regarding the BV value. In the design called SOI-pin6, small metal trenches connected to the aluminum contacts are also put inside the anode and cathode sides to pull-down the surface currents more into the SOI substrate, however, resulting BV was only 320 V.

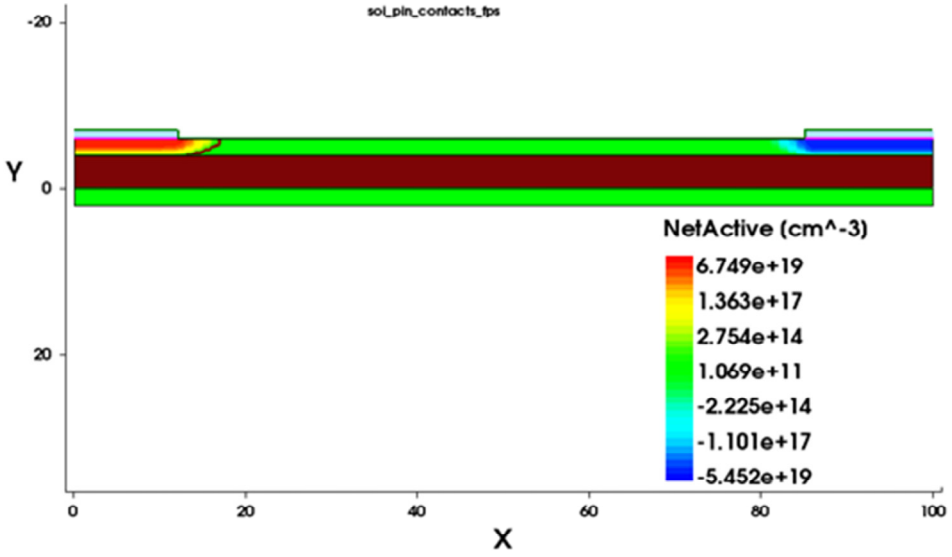


Fig.1. Sprocess simulation results of the design called SOI-pin5.

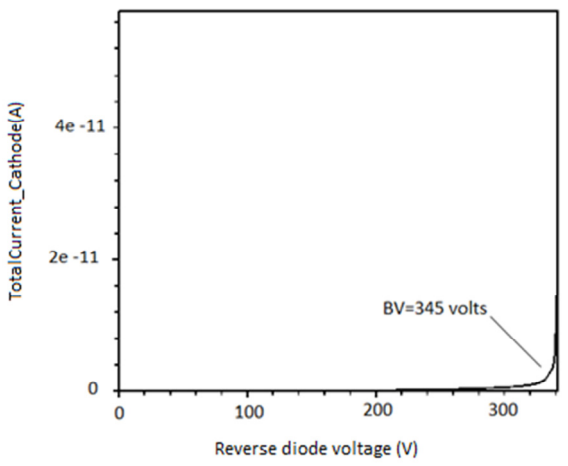


Fig. 2. BV plot of SOI-pin5 for 120 minutes final drive-in at 1050 degree C.

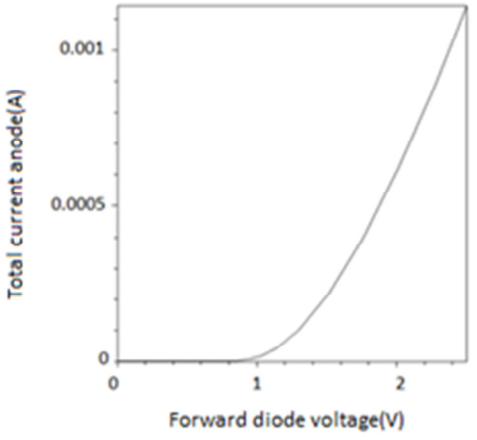


Fig. 3. I-V characteristic of the diode called SOI_pin5 under bias condition

2.2 SOI-pin6-thin results

Here, only the I-layer thickness in the design SOI-pin6 is reduced from 2 micron to 1 micron only. Fig. 4 shows the sproces result of SOI-pin6-thin. Unfortunately, the obtained BV value was only 300V. In fact, in the literature [13], it is indicated that the BV increases sharply with decreasing silicon thickness. This is a conflict result here.

After this experience, the slicon thickness is kept as 2 micron. But the oxide trench application was completely given up. Instead, three stepped lateral arsenic implant structure on the cathode side was applied. Before doing that, some process optimization works have been conducted on the SOI-pin5 since having BV of 345 V. The main purpose was to optimize the oxide thickness of the SOI substrate and timing of the annealing and drive in processes after N and P dopings. The design so called SOI-pin7 was for this purpose only.

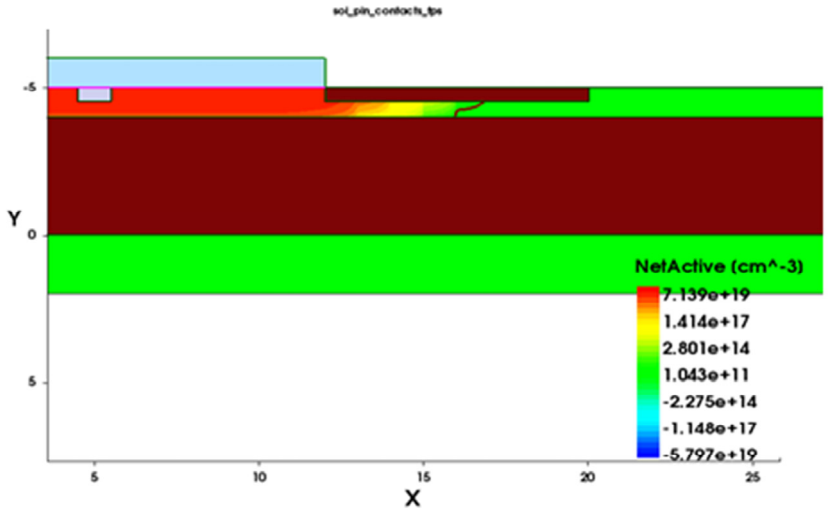


Fig..4. The sprocess simulation result of the design called SOI-pin6_thin.

2.3 SOI-pin7 results

First step:

The substrate oxide thickness was increased from 4 micron to 6 micron. The arsenic drive in was chosen as 30 minutes at 1000 degree C. The boron drive-in was chosen as 60 minutes at 1050 degree C. The BV value was relatively small, 140V. Therefore, increasing the substrate oxide thickness itself did not yield any improvement on BV value. Therefore, the drive-in durations were optimized. The arsenic drive-in was increased from 30 minutes to 120 minutes, and the boron drive-in was increased to 120 minutes. At the same time, the boron implant energy was also increased to 80 keV. The oxide thickness was kept as the same, 6 micron. These set values were resulted in more homogenous concentration profiles on the anode and the cathode sides. However, the resulting BV was only 290 V, which was not satisfying enough.

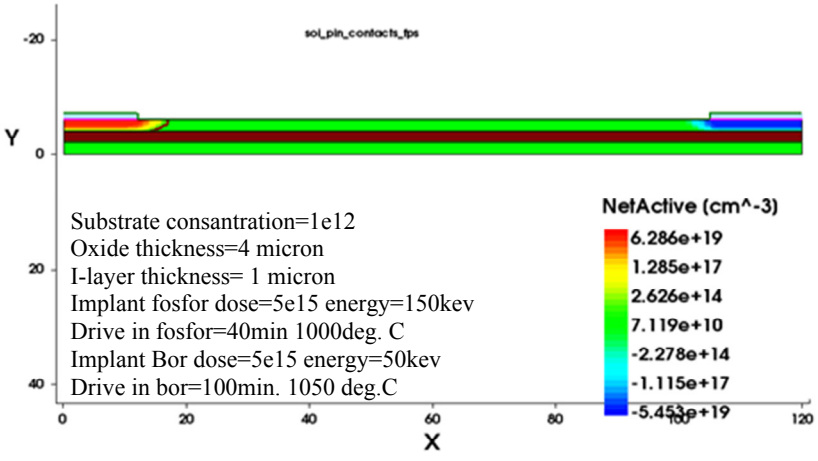


Fig. 5. The process simulation results of the design called “SOI-pin7”.

Second step:

In this case, the oxide thickness was reduced from 6 micron to 2 micron. But the other process parameters are kept the same. The resulting BV was 260 V only. As a result, it was decided that the oxide thickness of 4 micron was a good choice. The sprocess simulation result of the SOI-pin7 is given in Fig. 5. The next step was to apply the stepped implant on the cathode side of SOI-pin7 to obtain improvement.

2.4. The results of using stepped implant on the cathode side

In this design, three different dose amounts were chosen to form the stepped implant structure in lateral direction as shown in Fig. 6. Several sprocess and sdevice simulations were conducted to optimize the dose amounts. The resulting somewhat optimized dose amounts are listed below:

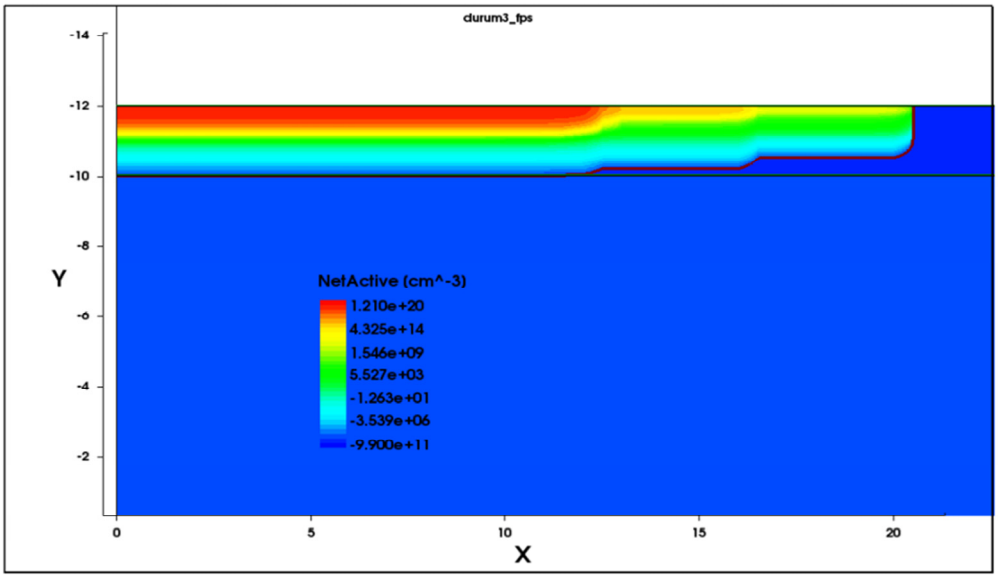


Fig. 6. Sprocess simulation result of the lateral stepped implant structure on the cathode side only (Note that only cathode side is focused on here)

N+ dose=5E15 cm^2 (the left most region of the arsenic implant)
N dose=2E14 cm^2 (the middle region of the arsenic implant)
N- dose=1E13 cm^2 (the right most region of the arsenic implant)

At the beginning, annealing duration chosen after each step implant process on the cathode side were chosen arbitrarily. Therefore, the obtained BV value was around 280 V only. After several trial and error sprocess simulations, annealing durations yielding the best result were decided as 15 minutes at the beginning, and final drive-in as 90 minutes. Finally, 480 V BV value was obtained. This result was relatively good as compared to earlier designs mentioned before. Therefore, these annealing and drive-in timing values were decided to keep in the later designs.

Later on, oxide trench application was tried again in the middle of the stepped implant and under one end of the aluminum cathode contact only as shown in Fig. 7. The resulting BV was 480 V. It was observed again that oxide trenches inside the substrate did not increase the BV value.

Finally, the RESURF technique with field plate, which is applied especially for high voltage LDMOS designs, was investigated from the literature [8], [11], [12]. The field plate usage between gate and drain contacts in LDMOS structures is adapted to the PIN design on SOI substrate here. An important amount of improvement on BV value was observed in this case. This can be considered as the main scientific contribution of this work.

In this structure, an oxide layer is horizontally placed on the surface of the I-layer and the aluminum cathode contact is extended on this oxide region forming a field plate as depicted in Fig. 8. The electrical field distributions inside the structure with and without RESURF technique applied are shown in Fig. 9, Fig. 10, and Fig. 11, Fig. 12. It is easily observed that the hot spots of the critical electric field distributions are relaxed or completely gone after RESURF technique with field plate usage. The resulting BV value is 600V, which is the best result when compared to earlier designs realized here.

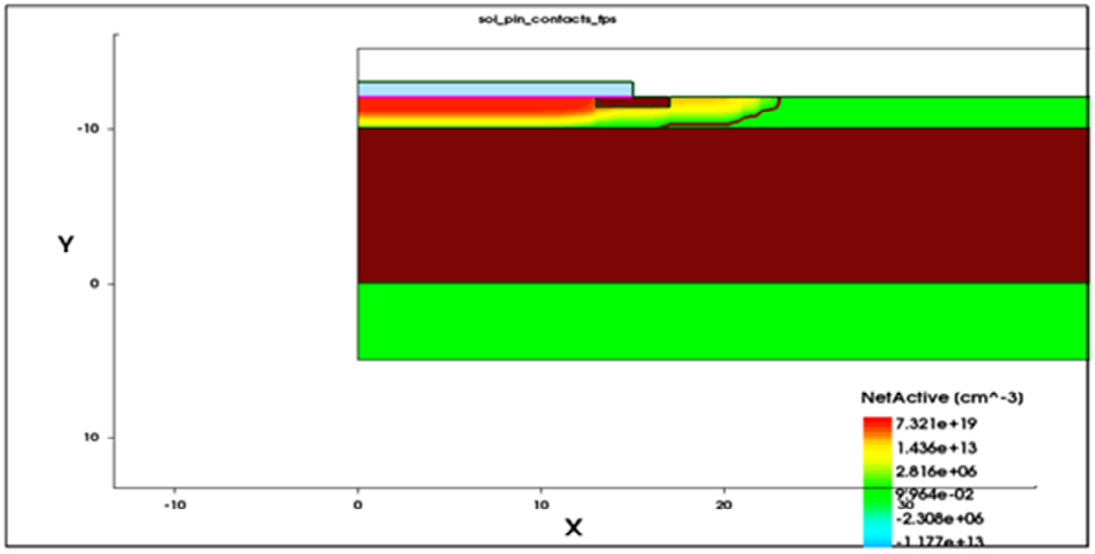


Fig. 7. Sprocess result of the stepped implant structure including oxide field plate on the cathode side only.

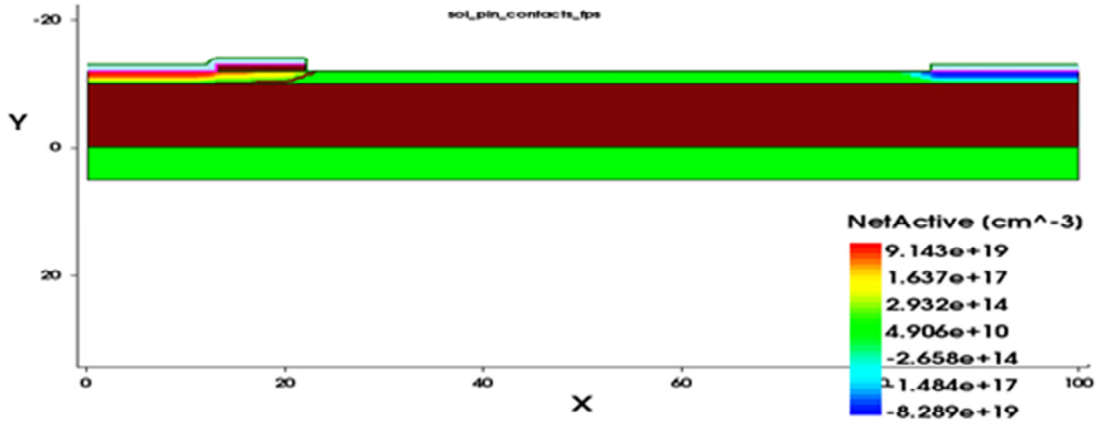


Fig. 8. The sprocess simulation result of the final design including RESURF technique with field plate.

The further studies to increase the BV value did not yield more than 600V of BV. In fact, the targeted BV value at the beginning of this research was to exceed 1000V. This aim has not been accomplished yet. Therefore, the study has been stopped at this point. However, it is believed that an applied reverse biased to the bottom of SOI substrate may increase the BV value further since it will form additional RESURF effect inside the SOI substrate. Namely, an additional depletion region extends inside the I-layer. Therefore, horizontal component of the breakdown voltage will be increased. This work will be done as a future work. The sprocess code belonging to the final design including the optimized critical fabrication parameters is also given the conclusion part.

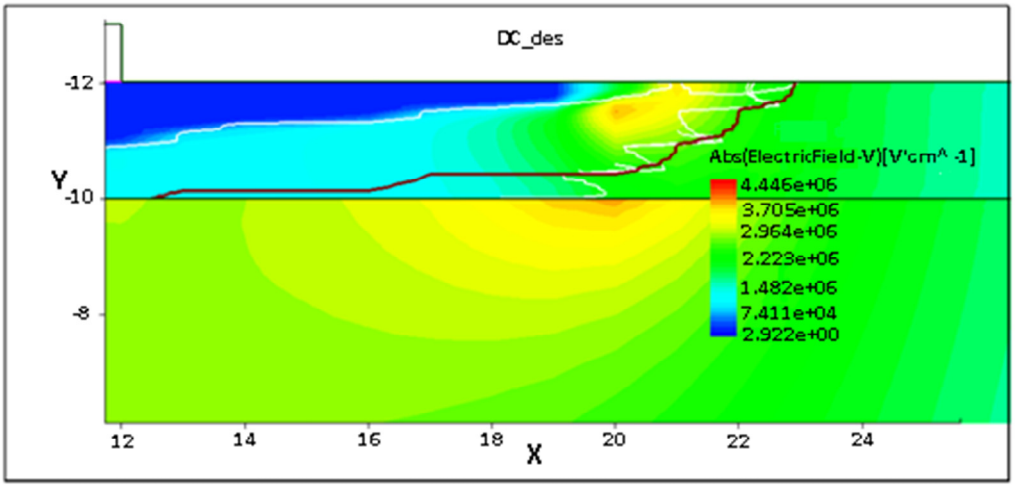


Fig. 9. Absolute E-Field distribution in the cathode side without RESURF technique.

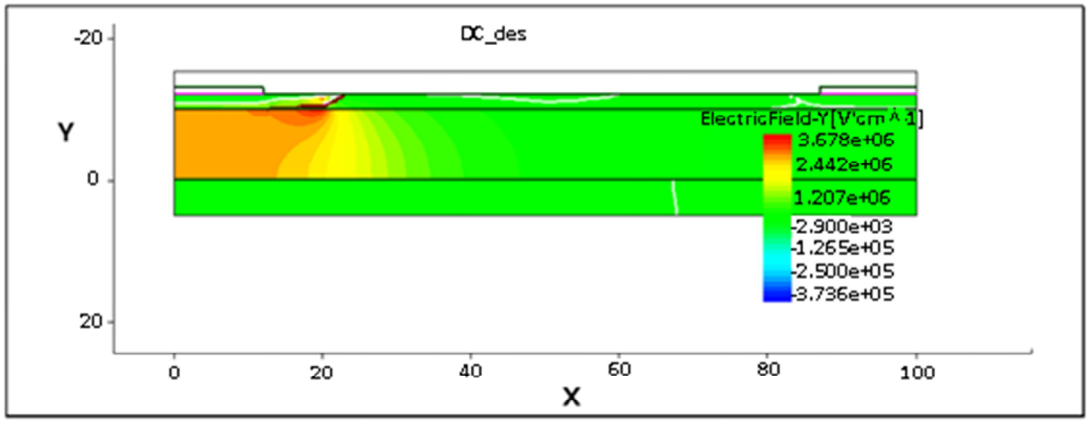


Fig. 10. E-field distribution on Y direction without RESURF technique (hot spots are seen easily).

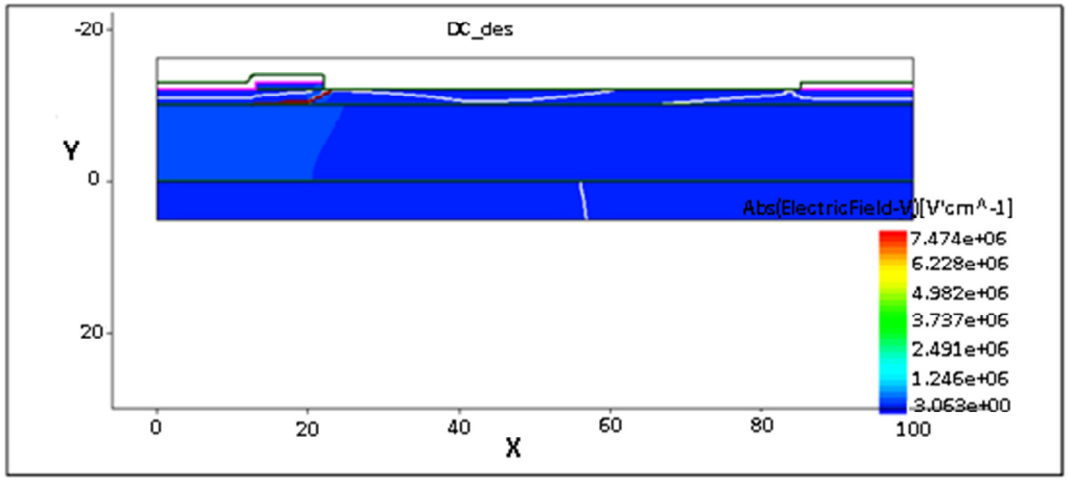


Fig. 11. Absolute E-Field distribution in the cathode side with RESURF technique (the yellow spots observed in Fig. 9 are removed here).

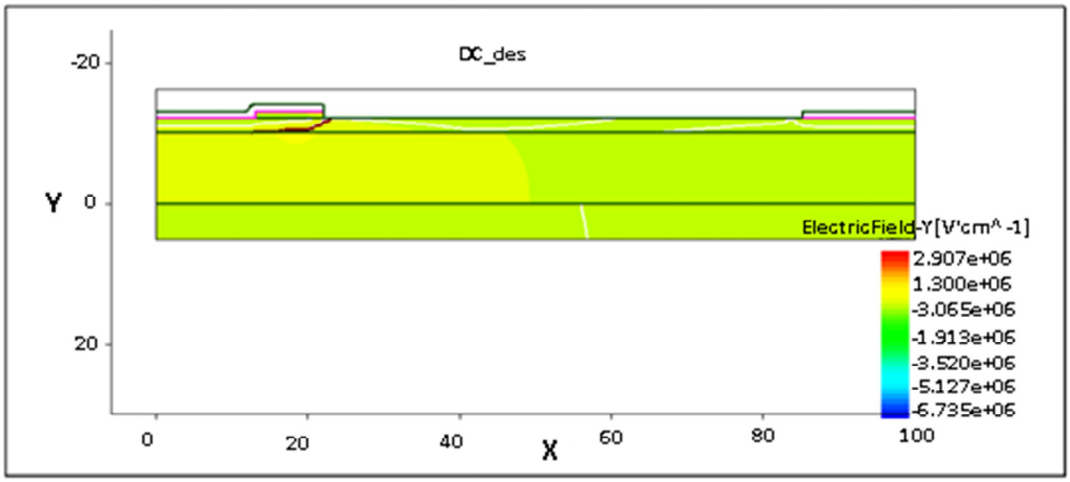


Fig. 12. E-field distribution on Y direction after RESURF technique (red hot spots are removed as seen easily).

3. Conclusion

In this work, A PIN diode design on SOI substrate for high voltage applications was realized using SENTAURUS TCAD platform. To increase the reverse breakdown voltage value of the PIN diode, several sprocess and sdevice simulations were conducted. Arsenic implant rather than phosphorus resulted in better result. In addition, a three stepped lateral arsenic implant on the cathode side increased the BV value. The geometrical optimizations were also completed as part of the investigation. The most recognized improvement was observed after using RESURF technique with field plate as is commonly used in LDMOS designs rather than high voltage diode designs in the literature. To ease the fabrication process, the bottom plate of the SOI substrate is not biased. However, A PIN diode design on an SOI substrate having 600 V of BV has been succeeded as shown in Fig. 13. It is believed that reverse biasing of the bottom plate will further increase the BV value. This work will be done as a future work. The final sprocess code of the PIN diode including the critical design parameters is given in Fig.14.

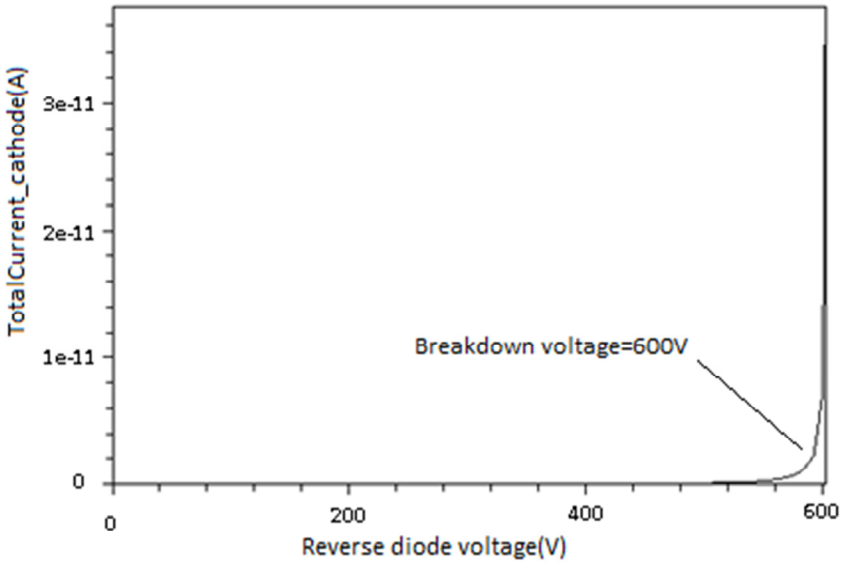


Fig. 13. I-V plot of the final PIN design under reverse bias indicating a BV of 600 V.

```
set sim_left 0
set sim_right 100
set sim_bottom 5
set sim_top 0
line y loc=0 spa=1  tag=left
line y loc=100 spa=1 tag=right
line x loc=-12 spa=0.1 tag=si_top
line x loc=-10 spa=0.1 tag=oxide_top
line x loc=0 spa=0.5 tag=top
line x loc=5 tag=bottom
region Silicon xlo=top xhi=bottom ylo=left yhi=right
region Oxide xlo=oxide_top xhi=top ylo=left yhi=right
region Silicon xlo=si_top xhi=oxide_top ylo=left yhi=right
init concentration=1e12 field=Boron wafer.orient=100
slice.angle=[CutLine2D 0 0 100.0 100.0]
#if {0} {
struct smesh=n@node0@
struct tdr=durum0
# forming n++ region
deposit material = {Oxide} type = isotropic  rate = {1.0} time=0.05
deposit material = {Photoresist} type = anisotropic  rate = {1.0}
time=1.5
mask name=mask_1_2 segments = {12 100} negative
photo mask=mask_1_2 thickness=1.5
etch material = {Photoresist} type=anisotropic rate = {1} time=1.5
implant Arsenic dose=2e15 energy=150 tilt=7 rot=-90
struct tdr=durum1
strip photoresist
strip oxide
temp_ramp name=tempramp_1_2 time=15 temp=1000
diffuse temp_ramp=tempramp_1_2
struct tdr=durum1.1
# forming n region
deposit material = {Oxide} type = isotropic  rate = {1.0} time=0.05
deposit material = {Photoresist} type = anisotropic  rate = {1.0}
time=1.5
mask name=mask_1_3 segments = {0 12 16 100} negative
photo mask=mask_1_3 thickness=1.5
etch material = {Photoresist} type=anisotropic rate = {1} time=1.5
implant Arsenic dose=5e14 energy=150 tilt=7 rot=-90
strip photoresist
strip oxide
temp_ramp name=tempramp_1_3 time=15 temp=1000
diffuse temp_ramp=tempramp_1_3
struct tdr=durum2
#forming n- region
deposit material = {Oxide} type = isotropic  rate = {1.0} time=0.05
deposit material = {Photoresist} type = anisotropic  rate = {1.0}
time=1.5
###continues on the next column###
```

```
mask name=mask_1_4 segments = {0 16 20 100} negative
photo mask=mask_1_4 thickness=1.5
etch material = {Photoresist} type=anisotropic rate = {1} time=1.5
implant Arsenic dose=1e14 energy=150 tilt=7 rot=-90
strip photoresist
strip oxide
struct tdr=durum3
#init tdr=durum3
temp_ramp name=tempramp_1_4 time=15 temp=1000
diffuse temp_ramp=tempramp_1_4
struct tdr=durum4
deposit material = {Oxide} type = isotropic  rate = {1.0} time=0.05
deposit material = {Photoresist} type = anisotropic  rate = {1.0}
time=1.5
mask name=mask_1_5 segments = {0 85} negative
photo mask=mask_1_5 thickness=1.5
etch material = {Photoresist} type=anisotropic rate = {1.5} time=1.1
struct smesh=n@node1@
struct tdr= durum5
#init tdr=durum5
implant Boron dose=5e15 energy=80 tilt=7 rot=-90
strip photoresist
strip oxide
temp_ramp name=tempramp_1_5 time=100 temp=1050
diffuse temp_ramp=tempramp_1_5
struct smesh=n@node2@
struct tdr= durum6
###Forming the RESURF section###
deposit material = {Oxide} type = anisotropic  rate = {1} time=0.9
deposit material = {Photoresist} type = anisotropic  rate = {1}
time=1.5
mask name=mask_1_6 segments = {13 25} negative
photo mask=mask_1_6 thickness=1.5
etch material = {Photoresist} type=anisotropic rate = {1} time=1.55
struct tdr= durum7
etch material = {Oxide} type=anisotropic rate = {1} time=0.9
struct tdr= durum8
strip photoresist
struct tdr= durum9
deposit material = {Aluminum} type = isotropic  rate = {1.0} time=1
struct tdr= durum10
mask name=mask_1_7 segments = {0 25 85 100} negative
photo mask=mask_1_7 thickness=1.5
etch material = {Aluminum} type=anisotropic rate = {1} time=2
strip Photoresist
struct tdr= durum11
contact name = "anode"   point  x = -12.5<um> y = 92<um>
contact name = "cathode"   point  x = -12.5<um> y = 6<um>
struct smesh=n@node@
struct tdr= soi_pin_contacts
exit
```

Fig.14. The final sprocess code of the SOI-PIN diode.

If the proposed structure here is compared to the work in [7], which is a similar work in terms of process technology except layer dimensions and resurf plate technique, it is seen that the DC breakdown voltage of 750 V is claimed. However, only a mathematical model is developed in [7]. Moreover, a very limited information is provided about the experimental verification of the developed model. Although the results presented here are not based on test results after real fabrication, they are surely more realistic than that of [7] since using very powerful process simulation tool, TCAD SENTAURUS SPROCESS. Hence, 600 V of DC breakdown voltage obtained here for a lateral SOI PIN diode can be accepted as a successful result.

References

[1] SKYWORKS Application Note-Design With PIN Diodes, SKYWORKS, pp. 1-19, 2002-2009. (http://www.skyworksinc.com/uploads/documents/200312C.pdf, (visiting date 20.07.2012)
[2]B. Doherty, "PIN Diode Fundamentals", MicroNote Series701, Microsemi Corporation. (http://www.microsemi.com/en/sites/default/files/micnotes/701.pdf, (visiting date 15.07.2012)
[3] www.microwavejournal.com/articles/print/20694-shunt-pin-diodes, (visiting date 24.07.2018)
[4] http://cdn.macom.com/datasheets/MADP-011029.pdf, (visiting date 24.07.2018)
[5] Z. J. Li, B. Zhang, X.R. Luo S.D. Hu, J. Fang, Z.H. Li, M. Qiao, Y. F. Guo, " The Rule of Field Enhancement for Buried Dielectric Layer of SOI High Voltage Devices", IEEE 2007 International Conference on Communications, Circuits and Systems, pp. 1302-1305, 2007
[6] S. Hu, Z. Li, B. Zhang, "Quantificational Dependence of Vertical Breakdown Voltage on Top Silicon and Dielectric Layer Thicknesses for SOI High Voltage Devices", IEEE 2008 International Conference on Communications, Circuits and Systems, pp. 1274-1277, 2008
[7] S. Merchant, E. Arnold, H. Baumgart, S. Mukherjee, H. Pein, and R. Pinker, "Realization of High Breakdown voltage (>700 V) in Thin SOI Devices", IEEE Proceedings of the 3rd International Symposium on Power Semiconductor Devices and ICs, pp 31-35, 1991.
[8] W.S. Son, Y.H. Sohn, S. Y. Choi, "SOI RESURF LDMOS transistor using trench filled with oxide", Electronics Letters, Vol.39, No.24, 2003
[9] T. Wang, X. Luo, " The Breakdown Characteristics of a New SOI High Voltage Device with Sandwich Buried Oxide Layer", 2009 IEEE International Conference on Communications, Circuits and Systems, pp.608-610, 2009
[10] Z. Li, Y. Guo, B. Zhang, J. Fang, Z. Li, "A New 2-D Analytical Model of Double RESURF in SOI High Voltage Devices", IEEE Proceedings 7th International Conference on Solid-State and Integrated Circuits Technology, pp. 328-331, 2004
[11] Q. Liu, Z. Li, B. Zhang, J. Fang, " The Research on Breakdown Voltage of High Voltage SOI LDMOS Devices With Shielding Trench", IEEE Proceedings 6th International Conference on Solid-State and Integrated Circuit Technology, pp.159-161, 2001
[12] V. Parthasarathy, V. Khemka, R. Zhu, A. Bose, " SOA Improvement by a RESURF LDMOS Technique in a Power IC Technology", IEEE International Electron Devices Meeting 2000. Technical Digest. IEDM, pp. 75-78, 2000
[13] S. Merchant, E. Arnold, M. Simpson, " Tunneling in Thin SOI High Voltage Devices" Proceedings of 1995 International Symposium on Power Semiconductor Devices & ICs, pp. 130-135, 1995